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Progress in Silicon Carbide Semiconductor Electronics Technology

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Silicon carbide's demonstrated ability to function under extreme high-temperature, high-power, and/or high-radiation conditions is expected to enable significant enhancements to a far-ranging variety of applications and systems. However, improvements in crystal growth and device fabrication processes are needed before SiC-based devices and circuits can be scaled-up and incorporated into electronic systems. This paper surveys the present status of SiC-based semiconductor electronics and identifies areas where technological maturation is needed. The prospects for resolving these obstacles are discussed. Recent achievements include the monolithic realization of SiC integrated circuit operational amplifiers and digital logic circuits, as well as significant improvements to epitaxial and bulk crystal growth processes that impact the viability of this rapidly emerging technology.

Key words: Power electronics, silicon carbide

INTRODUCTION

Silicon carbide (SiC) based semiconductor electronic devices and circuits are presently being developed for use in high-temperature, high-power, and/or high-radiation conditions under which conventional semiconductors cannot adequately perform. Silicon carbide's ability to function under such extreme conditions is expected to enable significant improvements to a far-ranging variety of applications and systems. These range from greatly improved high-voltage switching¹⁻³ for energy savings in public electric power distribution and electric vehicles to more powerful microwave electronics for radar and communications⁴ to sensors and controls for cleaner-burning more fuel-efficient jet aircraft and automobile engines.^{5,6} In the particular area of power devices,

theoretical appraisals have indicated that SiC power metal-oxide semiconductor field effect transistors (MOSFETs) and diode rectifiers would operate over higher voltage and temperature ranges, have superior switching characteristics, and yet have die sizes nearly 20 times smaller than correspondingly rated silicon-based devices.² However, these tremendous theoretical advantages have yet to be realized in experimental SiC devices. This is primarily due to the fact that SiC's relatively immature crystal growth and device fabrication technologies are not yet sufficiently developed to the degree required for reliable incorporation into electronic systems.

This paper surveys recent progress toward the realization of high temperature and/or high power SiC devices and circuits within the context of identifying specific performance-limiting areas where technological maturation is most needed. The prospects and possible time frame for the resolution of these

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Table I. Comparison of Selected Semiconductor Room Temperature Physical Properties

	<u>Si</u>	<u>GaAs</u>	<u>6H-SiC</u>	<u>4H-SiC</u>	<u>3C-SiC</u>
Bandgap (eV)	1.1	1.42	3.0	3.2	2.3
Breakdown Field @10 ¹⁷ cm ⁻³ (MV/cm)	0.6	0.6	3.2	3	>1.5
Electron Mobility @10 ¹⁶ cm ⁻³ (cm ² /V-s)	1100	6000	370	800	750
Saturated Electron Drift Velocity (cm/s)	10 ⁷	10 ⁷	2 × 10 ⁷	2 × 10 ⁷	2.5 × 10 ⁷
Thermal Conductivity (W/cm-K)	1.5	0.5	4.9	4.9	5.0
Hole Mobility @ 10 ¹⁶ cm ⁻³ (cm ² /V-s)	420	320	90	115	40
Commercial Wafers	12"	6"	1.375"	1.375"	None

crucial technological obstacles will also be discussed.

CRYSTAL GROWTH

Silicon carbide occurs in many different crystal structures (called polytypes) with each crystal structure having its own unique electrical and optical properties.^{7,8} The electrical properties of the more common SiC polytypes are compared to the properties of silicon and GaAs in Table I, which was constructed from data in Refs. 7 and 9–14. In many device applications, SiC's exceptionally high breakdown field (>5 times that of Si), wide band gap energy (>2 times that of Si), high carrier saturation velocity (2 times that of Si), and high thermal conductivity (>3 times that of Si) could lead to substantial performance gains, in spite of the low-field carrier mobility disadvantages.²

Although some of silicon carbide's superior intrinsic electrical properties have been known for decades, until recently there was a lack of SiC wafers with reproducible properties of sufficient electrical quality to realize advantageous devices and circuits. Efforts to solve the material shortage problem through the heteroepitaxial growth of 3C-SiC on large-area substrate materials (primarily silicon wafers) have not proven successful to date, as the resulting SiC material still contains too many defects to be useful.¹⁵ Only with the development of the modified Lely seeded sublimation growth technique have acceptably large and reproducible single-crystal SiC wafers of useable electrical quality become available.^{16–18} One-inch diameter 6H-SiC wafers first became commercially available in 1989,¹⁰ and the vast majority of silicon carbide semiconductor device technology development has taken place since that time.

Of the numerous polytypic forms of silicon carbide, 4H- and 6H-SiC electronic devices presently exhibit the most promise due to the availability and quality of reproducible single-crystal wafers in these polytypes. The size of commercially available 4H- and 6H-SiC wafers has recently been increased from 1 to 1.375 inches in diameter, and further up-scaling to 2 and 3 inch commercial wafer sizes is expected by the end of 1995 and 1997, respectively.¹³ Although Cree Research¹⁰ is the only U.S. company presently selling SiC wafers on the open market (prices in the neighborhood of US\$600–US\$2000 per wafer dependent on specifications), at least two other U.S. companies are

producing similar SiC wafers on a regular basis for internal purposes.^{19,20} If downward trends in wafer prices continue, SiC technology development should accelerate and expand as SiC research efforts become more affordable. Westinghouse recently reported two important firsts in SiC wafer growth: the attainment of semi-insulating SiC wafers with resistivities in excess of 10⁷ Ω-cm at room temperature and the realization of the first prototype 3 inch SiC wafers.²¹

4H-SiC's substantially higher carrier mobility compared to 6H-SiC¹¹ should make it the polytype of choice for most SiC electronic devices, provided that all other device processing, performance, and cost-related issues play out as being roughly equal between the two polytypes. Furthermore, the inherent mobility anisotropy that degrades conduction parallel to the crystallographic c-axis in 6H-SiC^{11,22} will particularly favor 4H-SiC for vertical power devices. Toward the end of minimizing parasitic substrate resistances in vertical power devices, 4H-SiC wafer resistivities as low as 0.0028 Ω-cm have recently been achieved.¹³ The emergence of higher mobility 4H-SiC has largely overshadowed significant progress made in obtaining greatly improved 3C-SiC through heteroepitaxy on low-tilt-angle 6H-SiC substrates.^{14,15} If on-going work ever solves the crystallographic defect problems associated with the heteroepitaxial growth of 3C-SiC on large-area silicon substrates, foundry compatibility and economic advantages would conceivably push 3C-SiC to the forefront.

The controlled growth of high-quality epilayers is naturally a key issue in the realization of SiC electronics. At present, the chemical vapor deposition (CVD) growth technique shows the most promise for attaining epilayer reproducibility and throughputs that will be required for mass production.²³ Homoepitaxial growth, whereby the polytype of the epilayer matches the polytype of the substrate, is accomplished by step controlled epitaxy, which is based upon growing on an SiC wafer polished at an angle of 3–4 degrees off the (0001) basal plane.^{24,25} This forces epilayer growth to take place at the abundance of growth surface steps so that the polytypic stacking sequence of the substrate is mirrored in the epilayer. In-situ doping is primarily accomplished through the introduction of nitrogen (usually N₂) for n-type and aluminum (usually trimethyl- or triethylaluminum)

for p-type gas species.

Recently, a major advancement which greatly enhances the range and control of in-situ doping of SiC during CVD growth was reported by Larkin et al.^{26,27} This technique, called site-competition epitaxy, has enabled reproducible doping concentrations low enough to enable the fabrication of the first 2 kV SiC rectifiers ever reported.²⁸ By growing the key n⁻ blocking voltage layer in a carbon-rich environment, most of the nitrogen present in the CVD system (whether it is a residual contaminant or intentionally introduced) is excluded from incorporating into the growing SiC crystal for the reason that the excess carbon species "out-competes" the nitrogen species for the carbon lattice site that nitrogen normally occupies when it dopes SiC. Kordina et al. have recently realized a record-breaking 4.5 kV SiC diode which was epitaxially grown in the carbon-rich environment of a graphite hot-wall CVD reactor.^{29,30} In contrast, by growing in a carbon-deficient environment, site competition epitaxy can instead be used to enhance the incorporation of nitrogen, so that heavily doped epilayers for ohmic contacts can be routinely produced when desired.

Improvements in epilayer uniformity and surface morphology will also be needed as SiC upscales from prototype devices toward production integrated circuits. Commercial epilayer thickness tolerance is presently specified at $\pm 25\%$,¹⁰ while researchers are reporting doping uniformities of $\pm 20\%$ and thickness uniformities of $\pm 7\%$ over a 2 inch wafer.²¹ Nonideal surface morphological features are readily observable on all homoepitaxial SiC films.³¹ The source and impact of these features on device performance is a topic of ongoing research. It is anticipated that technological maturation via refined CVD reactor designs and growth conditions will address these problems in the near future.

DISCRETE DEVICES

A variety of small-area prototype SiC devices has been reported in the literature in recent years,³²⁻³⁴ and some have already made their way into the marketplace. Blue light emitting diodes were the first silicon carbide based devices to reach high volume sales, while small signal diodes and junction field-effect transistor (JFETs) rated to 350°C and ultraviolet-sensitive photodiodes are more recently introduced commercial products.¹⁰ For the most part, early SiC devices have been produced using nonoptimized device designs and fabrication procedures. Only limited investigations into fundamental SiC device processing techniques, such as contact metallization, ion implantation, surface passivation, oxidation, and etching, have been carried out to date.³²⁻³⁴

In spite of the lack of optimized fabrication processes, some highly encouraging results, only some of which are specifically mentioned below, have been obtained from a variety of prototype SiC devices. The experimentally realized power performance of prototype X-band SiC metal semiconductor field-effect tran-

sistor (MESFETs) on highly parasitic low-resistivity substrates nevertheless exceeds the theoretical maximum power output density attainable in GaAs MESFETs at 1 GHz.^{35,36} The first microwave MESFETs fabricated on high resistivity 6H-SiC substrates attained a measured radio frequency gain of 8.5 dB at 10 GHz and an f_{\max} of 25 GHz.³⁷ Kimoto et al. recently demonstrated high voltage (500–1000 V) 4H-SiC Schottky rectifiers whose specific on-resistances are nearly 100 times smaller than the theoretical minimum on-resistances attainable in silicon Schottky diodes.³⁸ Operation of SiC p-n junction diodes, MOSFETs, MESFETs, JFETs, bipolar junction transistors (BJTs), and thyristors at temperatures above 300°C (and in some cases as high as 650°C) has been well established (Fig. 1).³²⁻³⁴ When these unpackaged devices are operated in atmospheric environments at temperatures near 600°C, chemical degradation of the contact metallizations restricts the functional lifetime to less than a few hours,³⁹ but much longer 600°C contact lifetimes have been demonstrated in inert nonoxidizing environments.⁴⁰ Clearly, reliable interconnection, passivation, and packaging technologies remain to be developed and proven before SiC devices can become truly useful in extreme high-temperature environments.

Given the extreme usefulness and success of MOSFET-based electronics in silicon, it is naturally desirable to implement high-performance inversion channel MOSFETs in SiC. Initial research results indicated that the quality of the SiO₂ formed by thermal oxidation of n-type 6H-SiC is comparable to oxides used for silicon MOSFETs, but oxides grown on p-type 6H-SiC exhibited poorer characteristics with substantially higher measured fixed charge and high interface state densities ($\sim 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$).^{41,42} High interface state densities, which have been attributed to the use of aluminum as the p-type dopant, natu-

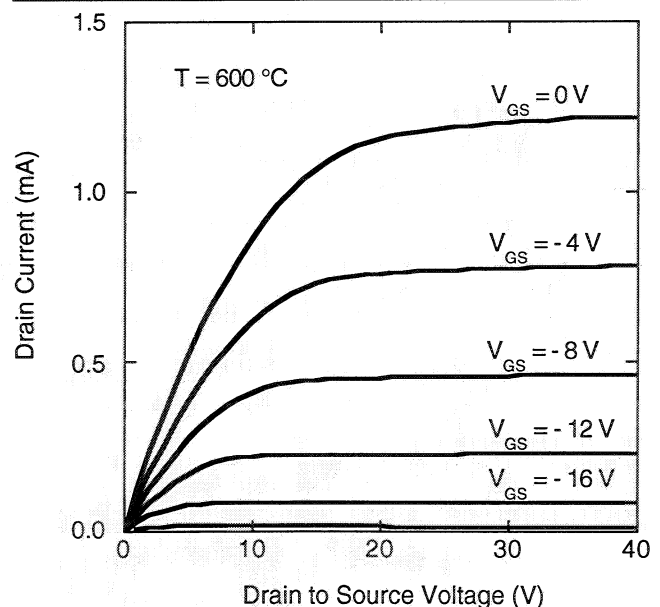


Fig. 1. Drain characteristics of a $10 \times 90 \mu\text{m}$ 6H-SiC buried-gate JFET at 600°C. After Ref. 39.

rally lead to low reported inversion channel electron mobilities that seriously degrade the performance of n-channel SiC MOSFETs.⁴¹⁻⁴³ However, on-going work toward better characterizing and improving the electrical quality of oxides on SiC offers encouragement that the predicted advantages of inversion channel SiC N-MOSFETs (especially vertical power SiC MOSFETs)² might be realized. In particular, Shenoy et al. have recently shown that more optimized oxidation procedures reduce interface state densities to around $2 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ in both aluminum-doped and boron-doped p-type 6H-SiC samples.⁴⁴ Since SiC devices will be operating at higher electric fields and temperatures than their silicon-based counterparts, very challenging oxide and surface passivation reliability issues will undoubtedly be faced as the technology progresses forward. The initial high-temperature reliability data collected to date indicates that

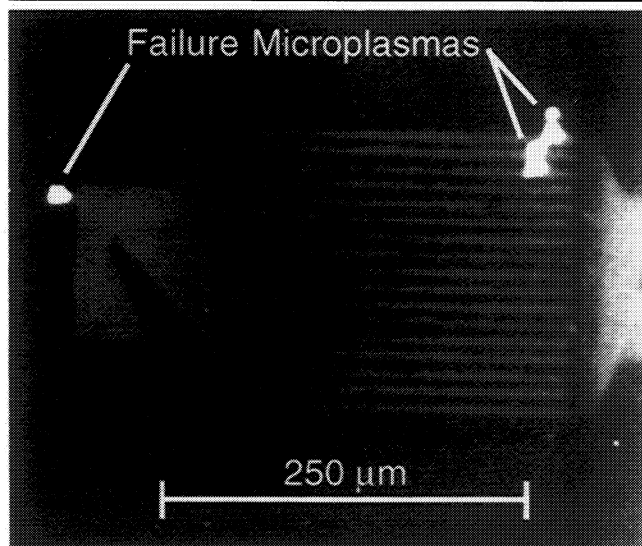


Fig. 2. Top view of highly localized microplasmas observed in the near-dark on a probing station as a 6H-SiC transistor fails due to the presence of micropipes.

SiC oxides need further development to become as reliable as optimized silicon thermal oxides at high temperature.⁴⁵ As the operational envelope of SiC is pushed toward increasingly extreme conditions, the development of dielectrics more robust than SiO_2 may become necessary.

Though many of the SiC devices described above exhibit very promising area-normalized electrical performances (i.e., A/cm^2 , W/mm , etc.), micropipe defects present in the SiC wafers (which propagate into subsequently grown homoepilayers)⁴⁶ prevent small-area prototype power device results from being scaled-up into useful large-area ($>1 \text{ mm}^2$), multi-amp power devices.⁴⁷ The micropipe defects, which are typically present in densities of a few hundred per square centimeter, generally lead to junction breakdown at electric fields well below the known critical-field. Figure 2 shows an optical micrograph of localized microplasmas associated with premature reverse-bias failure at micropipes in a 6H-SiC transistor. The origin of these defects is still very much a topic of current debate and research,⁴⁸⁻⁵¹ but their density has been steadily decreasing at a roughly twofold rate every year to a present-day minimum density of 55 per square centimeter.¹³ Further rapid progress toward eradicating these defects is expected, as Cree Research has speculated that micropipe densities can be rapidly decreased over the next few years and possibly eliminated in four to five years.¹³

In addition to micropipe defects, the density of dislocation defects in SiC wafers and epilayers has been measured^{48,49} on the order of $10,000 \text{ cm}^{-2}$. These defects are not nearly as detrimental to device performance as micropipes, because if they were, almost none of the attractive prototype SiC devices reported to date would have been possible. However, it remains to be ascertained what "secondary" effects the dislocations are having on leakage currents, breakdown processes, carrier lifetimes, and other physical device phenomena. The fact that areas larger than 1 mm^2

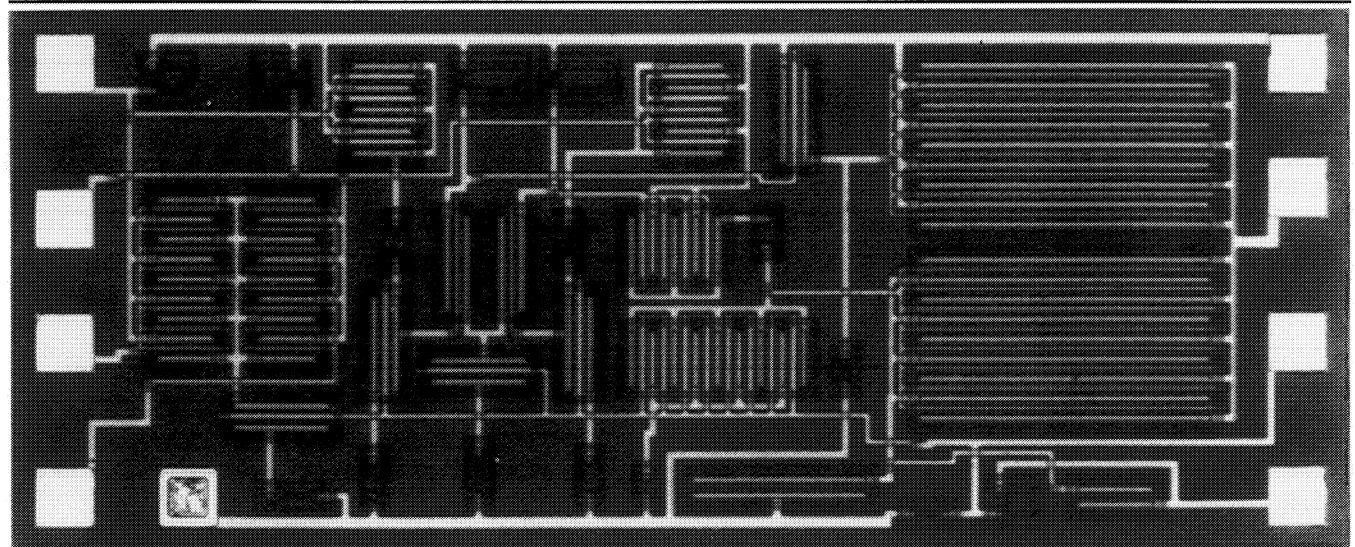


Fig. 3. Photomicrograph of SiC MOSFET operational amplifier chip. The chip size is $1 \times 2 \text{ mm}$. After Ref. 45. (Courtesy of D.M. Brown, General Electric Company)

within SiC Lely-platelet crystals (which are not considered suitable for mass production) have been observed to be totally free of dislocations and micropipes⁴⁸ suggests that these defects are preventable.

INTEGRATED CIRCUITS

Although they have a severe impact on high-field power devices, the micropipes appear to be less of a problem for signal-level electronics where devices are operated at much lower electric fields. This is evidenced by the recent achievement of Brown and coworkers at General Electric, who successfully fabricated the first complete monolithic integrated SiC operational amplifier chips.⁴⁵ The 1×2 mm 6H-SiC op-amp chip shown in Fig. 3 exhibited yields far higher than could be expected if micropipes were fatal to the active devices in this low-voltage circuit. Based on highly conservative 7 μ m design rules, the packaged circuit demonstrated 49 to 54 dB gains and bandwidths of 724 kHz to 269 kHz as temperature increased from 25 to 300°C. The chip was based on depletion mode n-channel MOSFET technology,⁵² which alleviated the low effective carrier mobilities in inversion channel SiC N-MOSFETs.

Despite the fact that SiC thermal oxides have not yet been optimized, Xie and coworkers at Purdue University recently demonstrated SiC digital integrated circuits based on inversion channel N-MOSFETs.^{53,54} Basic digital logic gates, latches, flip-flops, binary counters, and half adder circuits with up to a dozen transistors were fabricated and successfully operated over the temperature range from 25 to 300°C. These circuits are envisioned as first-generation prototypes for on-chip peripheral logic to drive one-transistor nonvolatile random access memory (NVRAM) arrays,⁵⁵ but clearly demonstrate the present feasibility of small SiC digital integrated circuits.

It is anticipated that increasingly larger digital and analog integrated circuits will be demonstrated in the near future. The functional sizes and yields of these circuits will probably be influenced by the aforementioned crystal growth uniformity and defect issues. As crystal growth limitations are resolved, however, device and packaging reliability issues could well become the primary factor limiting the capabilities and use of high-temperature SiC integrated circuits. Much work remains to be done in this area, since very little SiC device and packaging reliability data has been reported to date.

SUMMARY

Although the advantageous properties of SiC have been known for decades, it was largely an enabling technical breakthrough in crystal growth that made mass production of useful SiC semiconductor devices and circuits seem possible. This, coupled with an acknowledged growing need for high temperature electronics, has led to SiC's accelerated development over the last half-decade. Although progress to date has yielded a few products and highly encouraging

prototype results, some crucial technical obstacles remain to be solved before SiC can achieve its true potential. It is of paramount importance that crystal growth continue to improve, as larger wafers with far lower defect densities and improved epilayer doping and thickness control will be required for the majority of envisioned SiC electronic products. When combined with the continued maturation of device processing and high temperature packaging technologies, an increasingly capable variety of SiC devices and circuits will evolve to meet the system demands for hostile-environment electronics.

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